FIG. 1

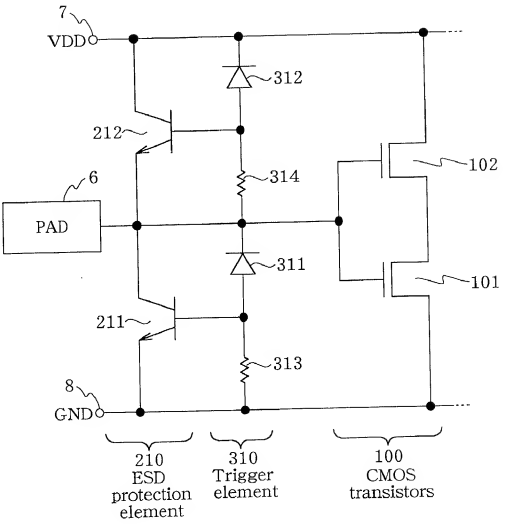

7
VDD
312
212
102
6
314
PAD
311
101
211
313
8
GND
210
ESD
protection
element
310
Trigger
element
100
CMOS
transistors

FIG.2

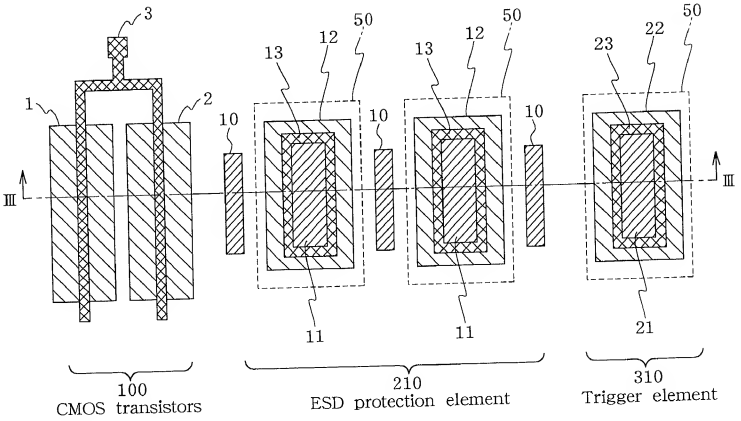


FIG.3

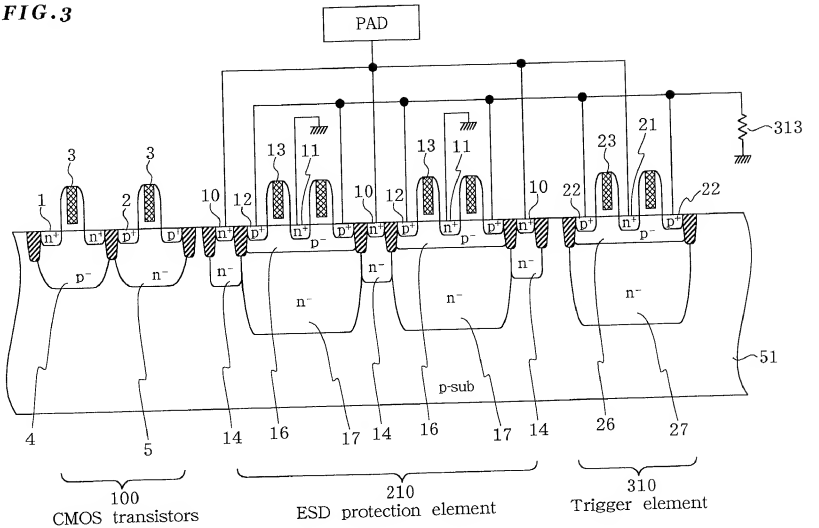

PAD
313
3
3
1
2
10
12
13
11
10
12
13
11
10
23
21
22
22
n+
p+
p-
n-
51
p-sub
4
5
14
16
17
14
16
17
14
26
27
100
CMOS transistors
210
ESD protection element
310
Trigger element

FIG.4

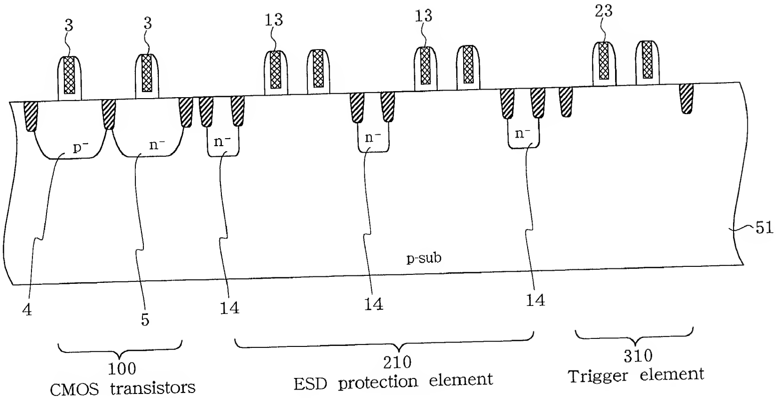

3
3
13
13
23
p⁻
n⁻
n⁻
n⁻
n⁻
p-sub
51
4
5
14
14
14
100
CMOS transistors
210
ESD protection element
310
Trigger element

FIG.5

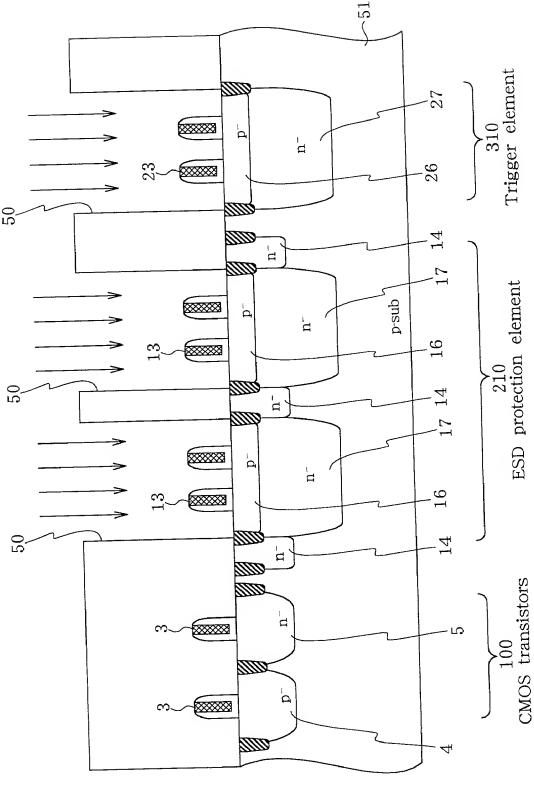

50
51
3
4
5
13
14
16
17
23
26
27
p-sub
100
CMOS transistors
210
ESD protection element
310
Trigger element

FIG.6

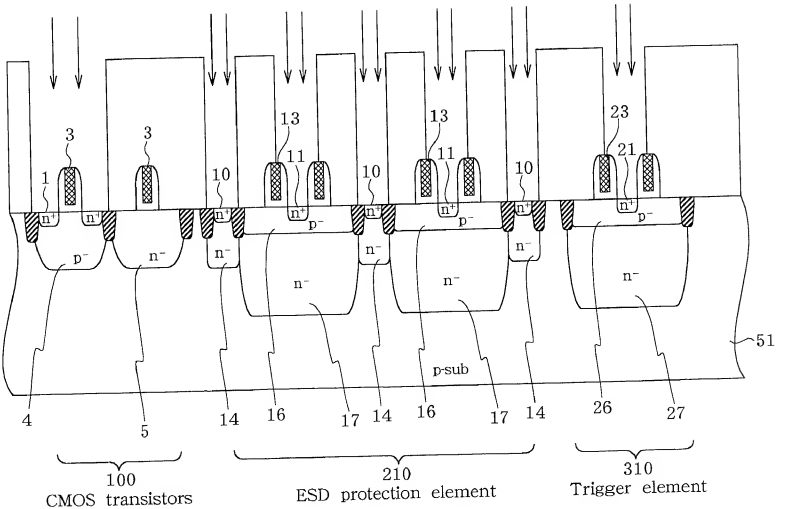
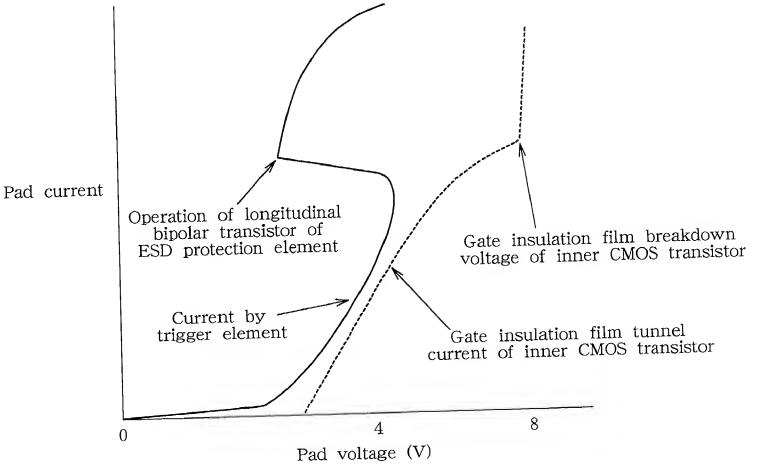


FIG. 7



Operation voltage of longitudinal bipolar transistor < gate insulation film breakdown voltage of inner CMOS transistor

FIG.8

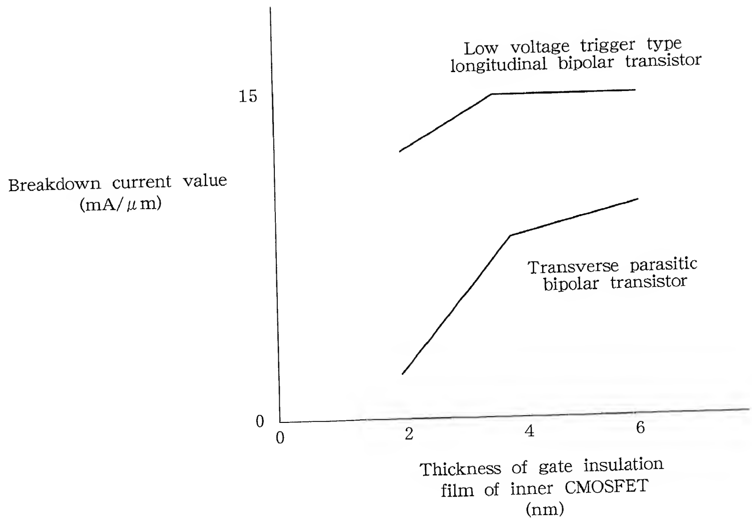

Low voltage trigger type longitudinal bipolar transistor
Transverse parasitic bipolar transistor
Breakdown current value (mA/μm)
15
0
0
2
4
6
Thickness of gate insulation film of inner CMOSFET (nm)

FIG. 9

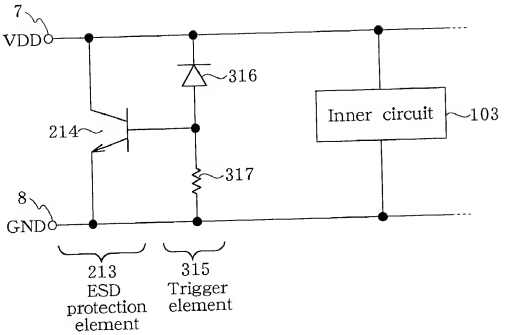

7
VDD
316
214
Inner circuit
103
317
8
GND
213
ESD
protection
element
315
Trigger
element

FIG.10

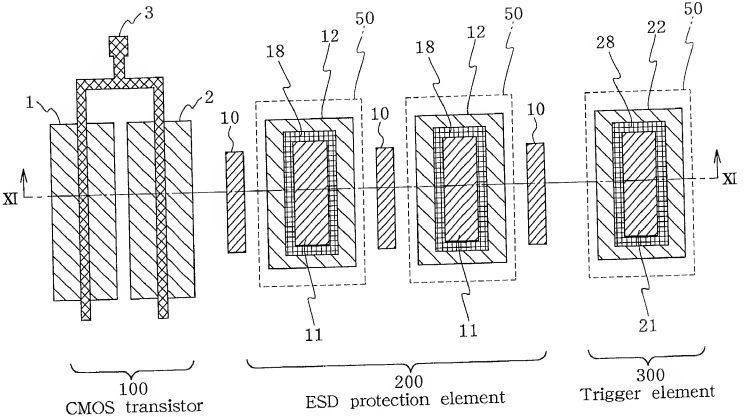

3
1
2
XI
10
18
12
50
11
100
CMOS transistor
200
ESD protection element
28
22
21
300
Trigger element

FIG.11

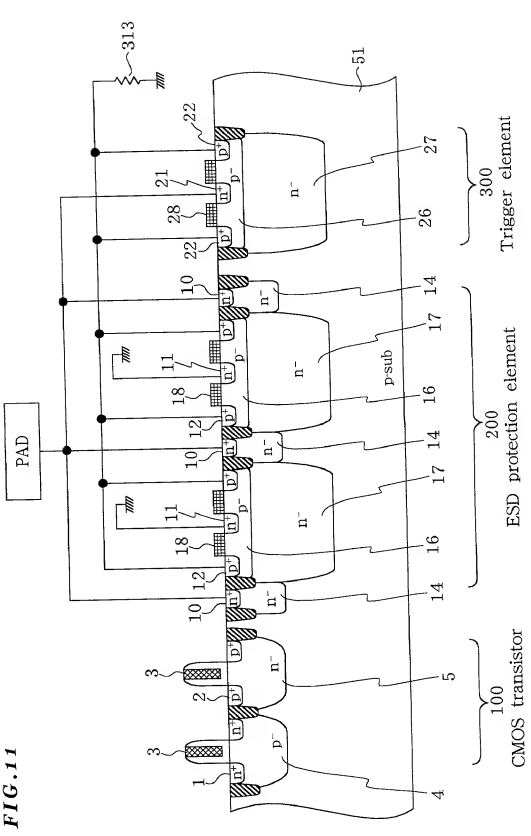


FIG.12

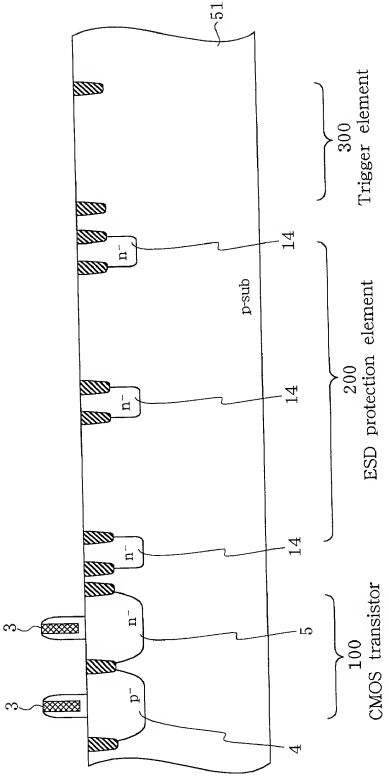

51
3
3
p⁻
n⁻
n⁻
n⁻
n⁻
p-sub
4
5
14
14
14
14
100
CMOS transistor
200
ESD protection element
300
Trigger element

FIG.13

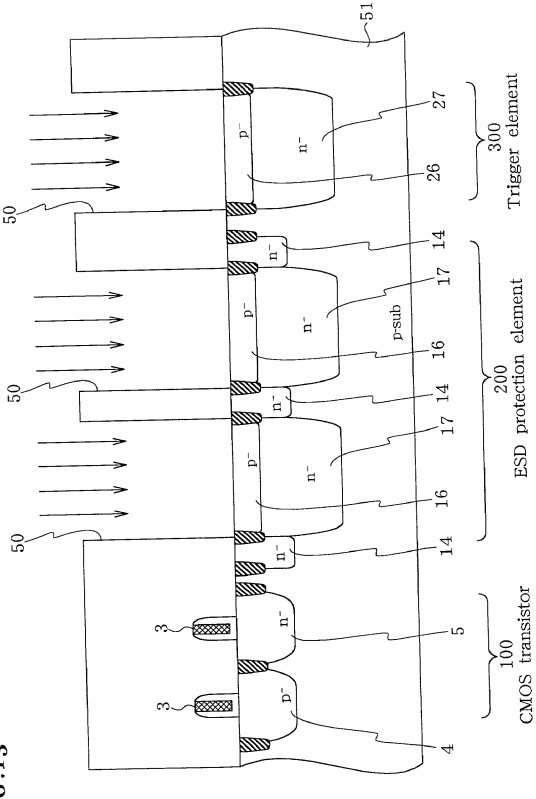

50
50
50
51
3
3
n⁻
p⁻
n⁻
p⁻
n⁻
p⁻
n⁻
p⁻
n⁻
p⁻
n⁻
p⁻
n⁻
p-sub
4
5
14
16
17
14
16
17
14
26
27
100
CMOS transistor
200
ESD protection element
300
Trigger element

FIG.14

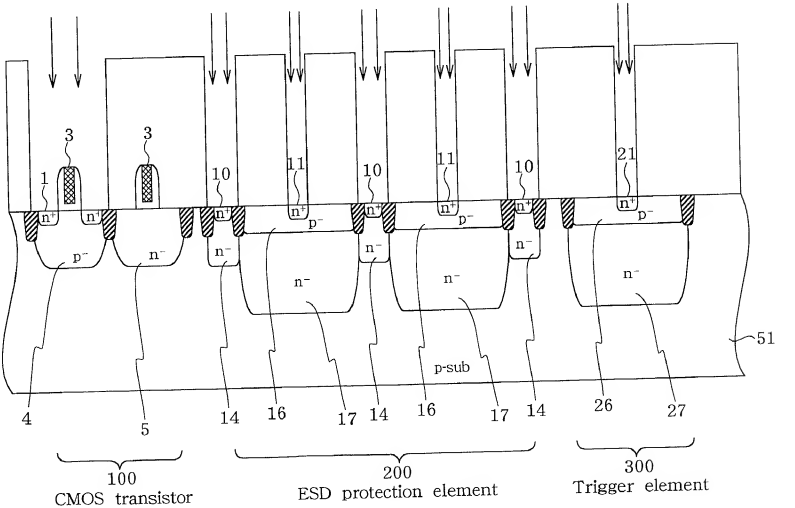


FIG.15

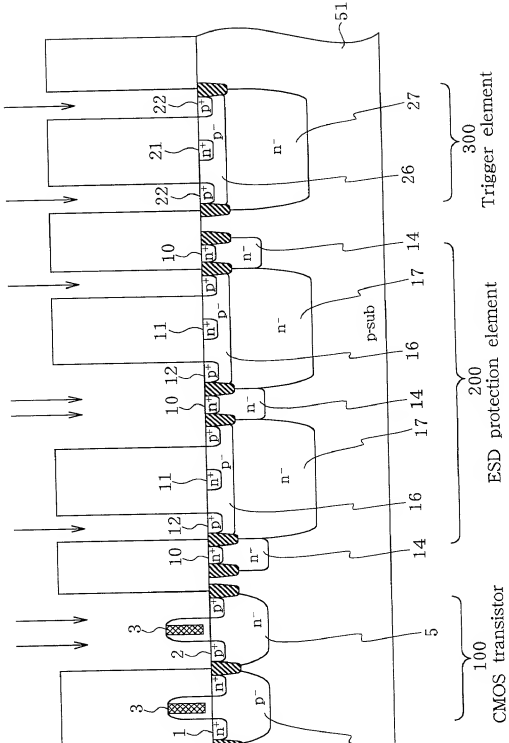


FIG.16

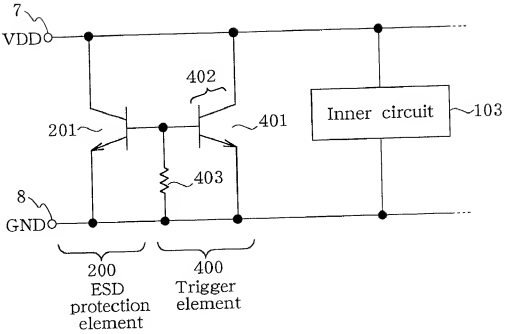

7
VDD
402
201
401
Inner circuit
103
403
8
GND
200
ESD
protection
element
400
Trigger
element

FIG.17

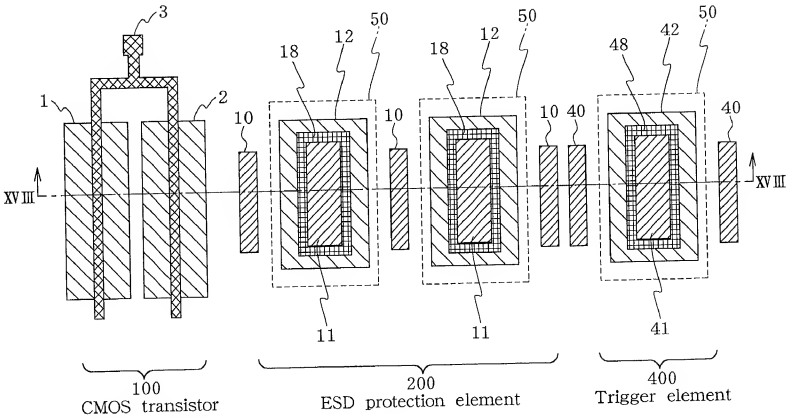


FIG.18

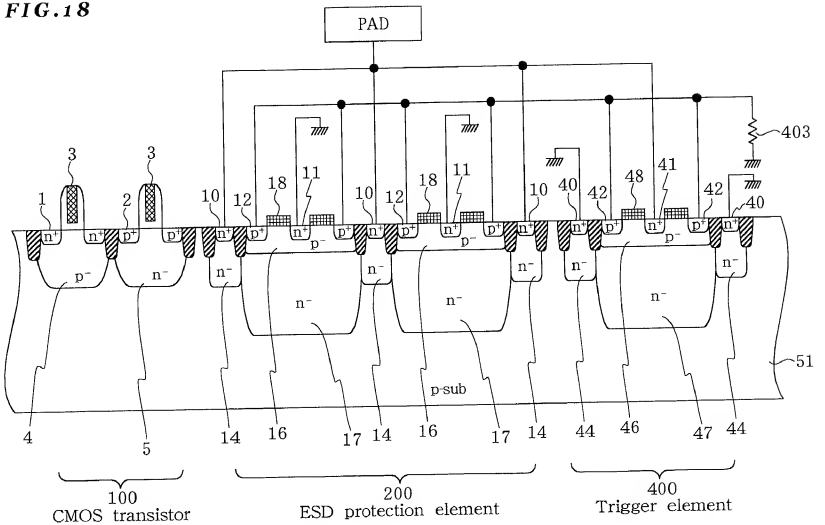


FIG.19

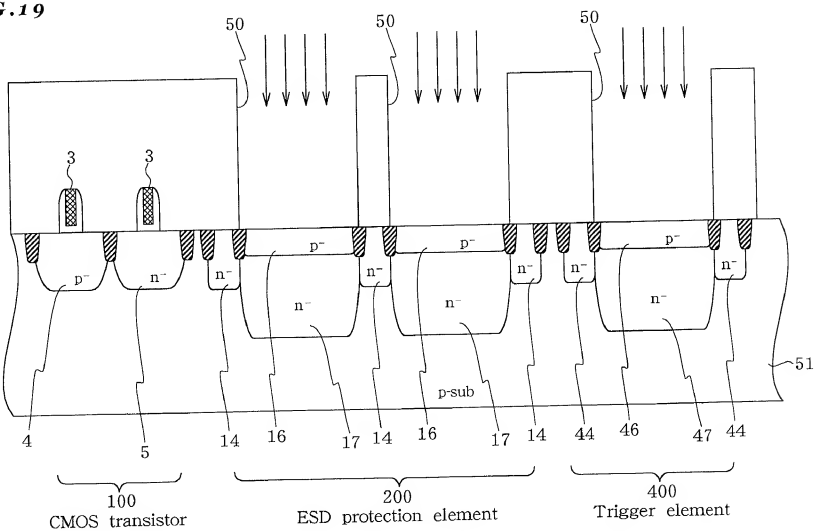


FIG.20

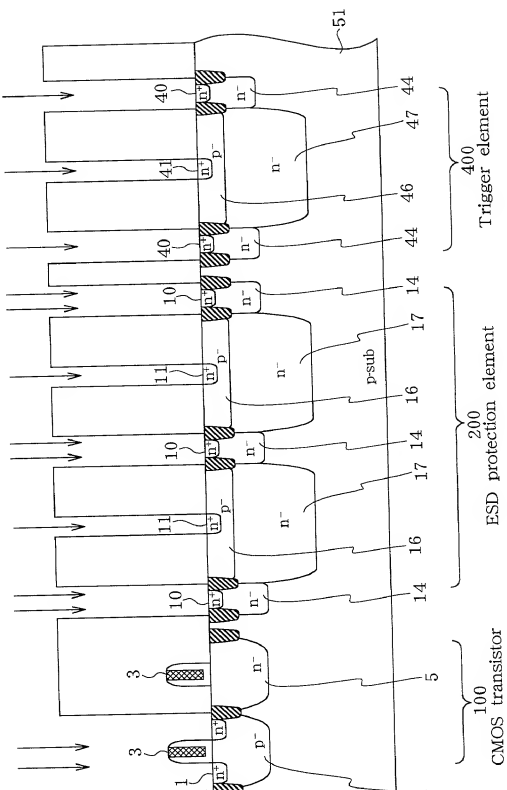

51
1
3
3
4
5
10
10
10
11
11
14
14
14
16
16
17
17
40
40
41
44
44
46
47
n+
p+
n-
p-
p-sub
100
CMOS transistor
200
ESD protection element
400
Trigger element

FIG.21

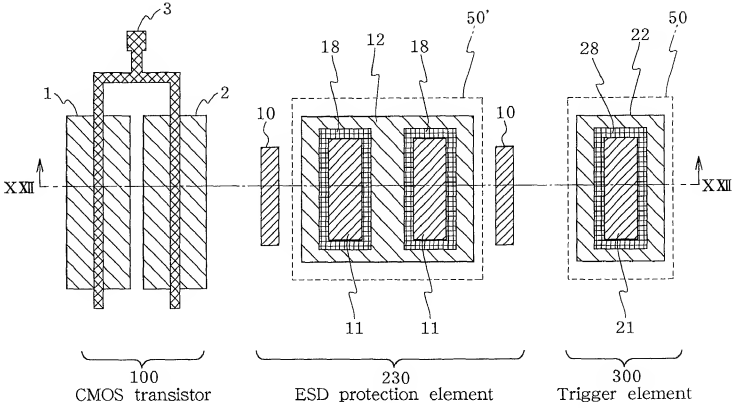

3
1
2
10
18
12
18
50'
10
28
22
50
XXII
XXII
11
11
21
100
CMOS transistor
230
ESD protection element
300
Trigger element

FIG.22

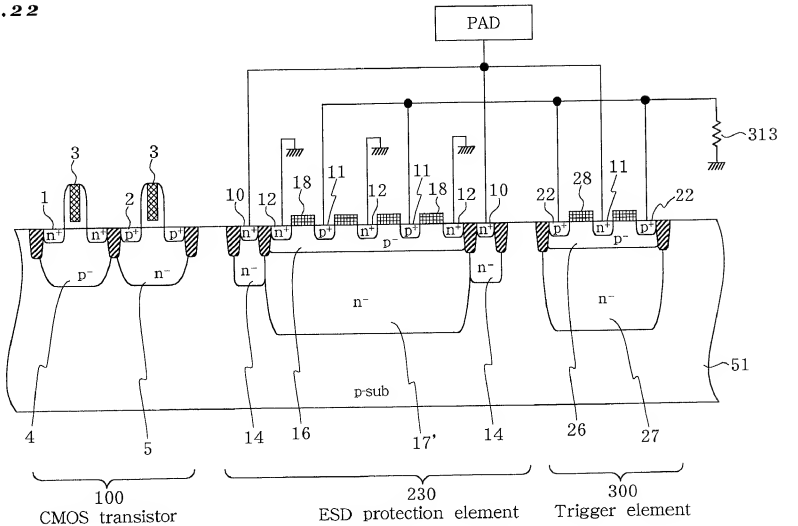

PAD
313
3
3
1
2
10
12
18
11
12
11
18
12
10
22
28
11
22
n+
p+
p-
n-
51
p-sub
4
5
14
16
17'
14
26
27
100
CMOS transistor
230
ESD protection element
300
Trigger element

FIG.23

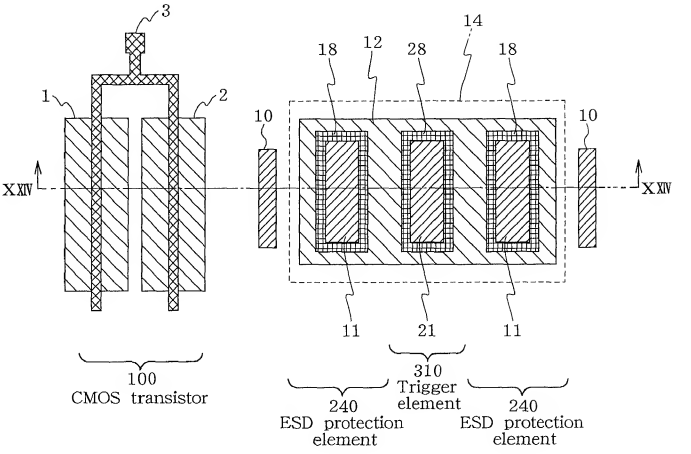

3
1
2
XIV
XIV
10
10
18
12
28
14
18
11
21
11
100
CMOS transistor
310
Trigger element
240
ESD protection element
240
ESD protection element

FIG.24

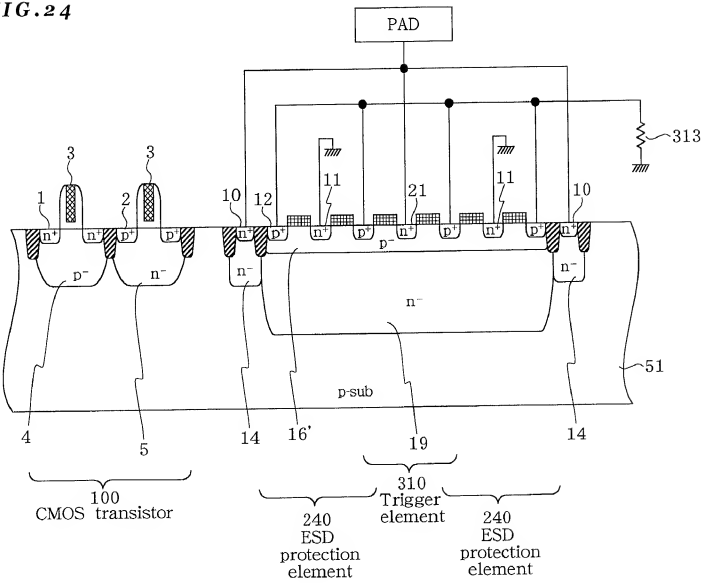

PAD
313
3
3
1
2
10
12
11
21
11
10
n+
p+
p-
n-
51
p-sub
4
5
14
16'
19
14
100
CMOS transistor
240
ESD
protection
element
310
Trigger
element
240
ESD
protection
element

FIG.25

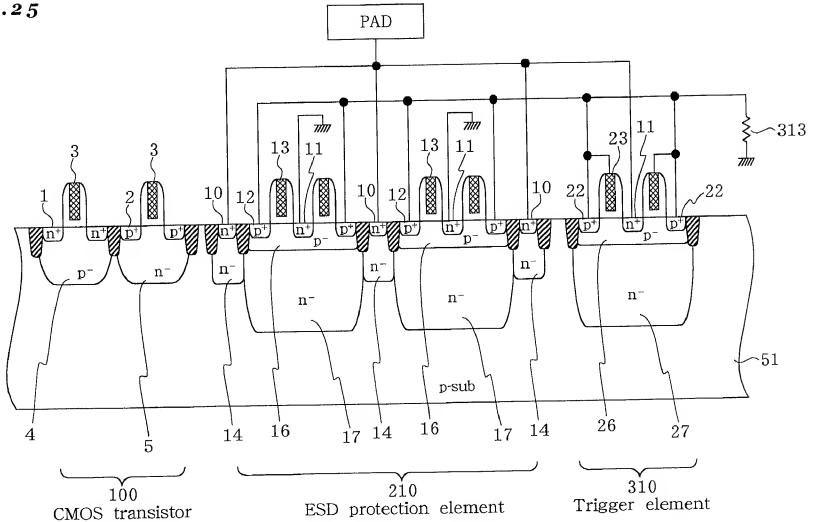


FIG.26

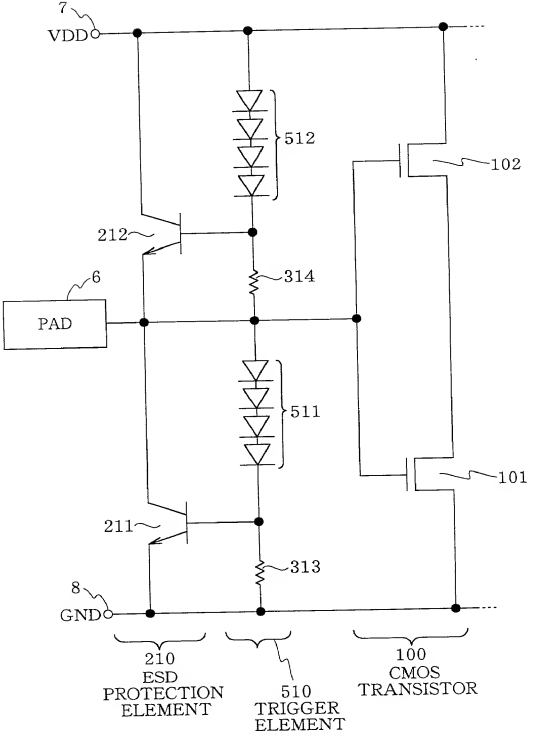

7
VDD
512
102
212
6
314
PAD
511
101
211
313
8
GND
210
ESD
PROTECTION
ELEMENT
510
TRIGGER
ELEMENT
100
CMOS
TRANSISTOR

FIG.27

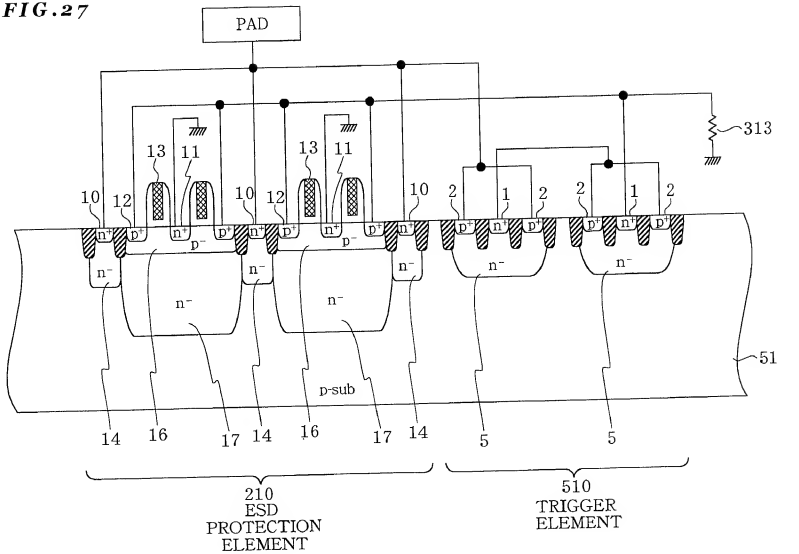

PAD
313
13
11
10
12
2
1
n+
p+
p-
n-
p-sub
51
14
16
17
5
210
ESD
PROTECTION
ELEMENT
510
TRIGGER
ELEMENT

FIG.28

COMPARISON OF FORWARD SERIES CONNECTION DIODE AND INVERSE DIODE

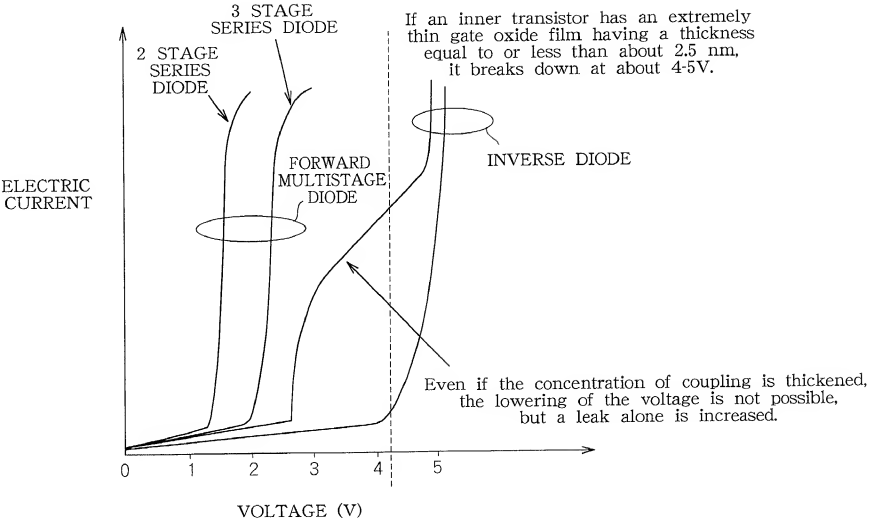


FIG.29

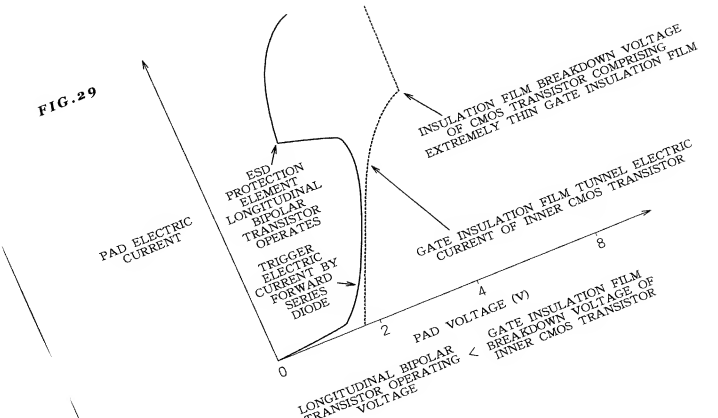

PAD ELECTRIC CURRENT
ESD PROTECTION ELEMENT LONGITUDINAL BIPOLAR TRANSISTOR OPERATES
TRIGGER ELECTRIC CURRENT BY FORWARD SERIES DIODE
INSULATION FILM BREAKDOWN VOLTAGE OF CMOS TRANSISTOR COMPRISING EXTREMELY THIN GATE INSULATION FILM
GATE INSULATION FILM TUNNEL ELECTRIC CURRENT OF INNER CMOS TRANSISTOR
0
2
4
8
PAD VOLTAGE (V)
LONGITUDINAL BIPOLAR TRANSISTOR OPERATING VOLTAGE
<
GATE INSULATION FILM BREAKDOWN VOLTAGE OF INNER CMOS TRANSISTOR

FIG.30

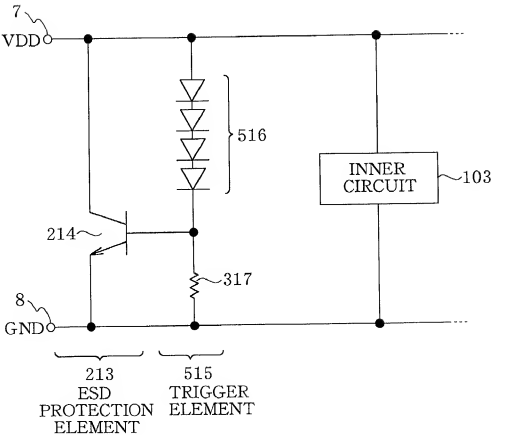

7
VDD
516
INNER
CIRCUIT
103
214
317
8
GND
213
ESD
PROTECTION
ELEMENT
515
TRIGGER
ELEMENT

FIG.31

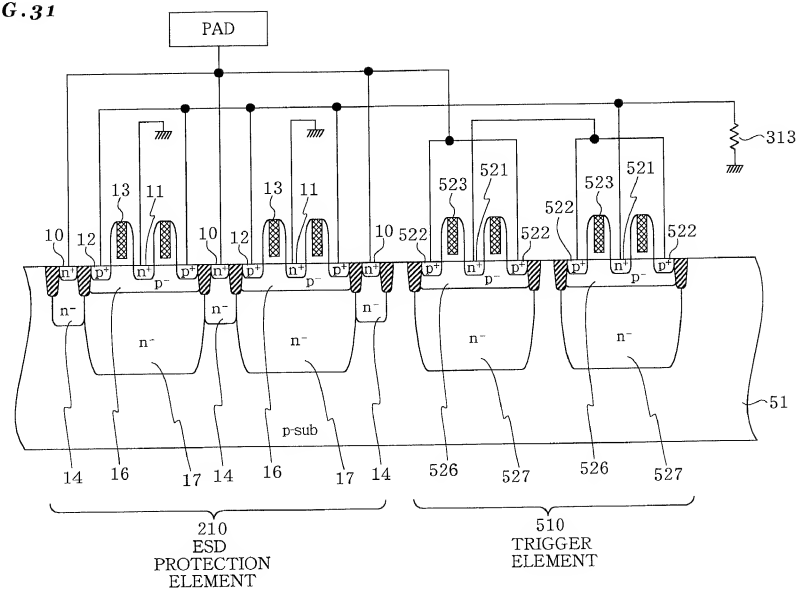

PAD
313
13
11
523
521
522
10
12
p+
n+
p-
n-
51
p-sub
14
16
17
526
527
210
ESD
PROTECTION
ELEMENT
510
TRIGGER
ELEMENT

FIG.32(a)

DIODE COMPRISING
p+LAYER/ n well
FABRICATED BY
EXISTING CMOS PROCESS

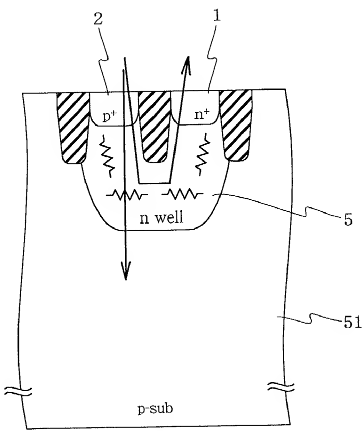


FIG.32(b)

DIODE UTILIZING ONE PORTION
OF LONGITUDINAL
BIPOLAR TRANSISTOR

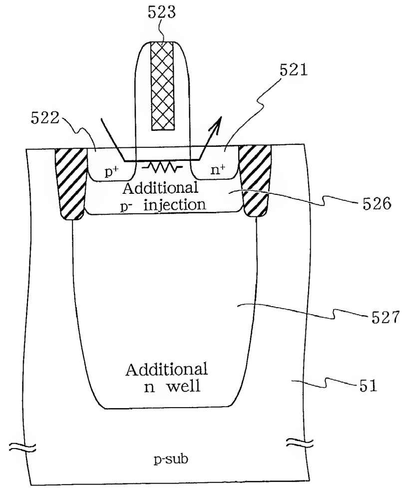
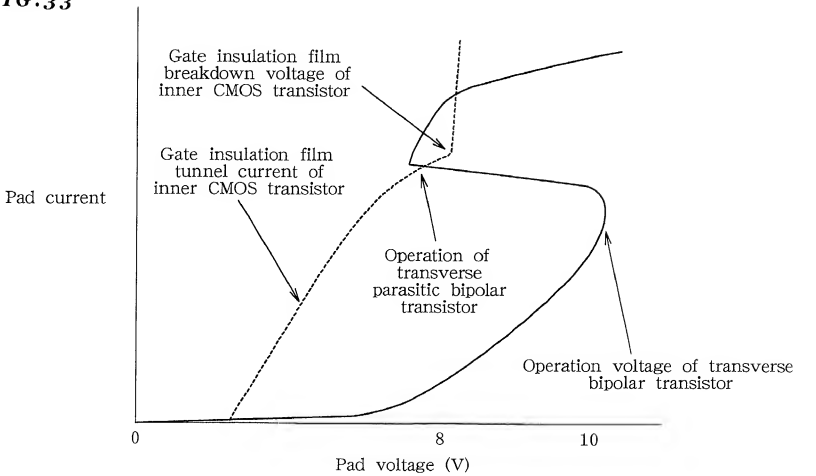


FIG.33



Operation voltage of transverse bipolar transistor < gate insulation film breakdown voltage of inner CMOS transistor